IN THE CLAIMS:

1. (Canceled)

2. (Currently Amended) A multiple-format video encoder as claimed in claim ~~1~~ 13,

wherein the address calculating circuit comprises:

a value selecting circuit for ~~selecting a predetermined~~ calculating the value to be added ~~in accordance with the video format actually used~~;

an adder for adding the value to be added ~~selected~~ calculated by the value selecting circuit to the address ~~addresses specified~~ designated by the address calculating circuit and outputting a value thus obtained; and

a flip-flop circuit for temporarily storing the value ~~values~~ output from the adder and refreshing ~~those values~~ this value in synchronism with regular clock pulses so ~~that the addresses are refreshed with those values~~ as to output the value therefrom.

3. (Canceled)

4. (Currently Amended) A multiple-format video encoder as claimed in claim ~~1~~ 13,

wherein the color-difference signal includes color-difference signals B-Y and R-Y,

wherein the trigonometric function values ~~of the trigonometric functions~~ include values of sine and cosine functions, and

wherein the ~~multiplying circuit~~ multiple-format video encoder further comprises:

a first multiplying circuit for multiplying the color-difference signal B-Y by the values of the sine function;

a second multiplying circuit for multiplying the color-difference signal R-Y by values calculated from the values of the cosine function; and

an adding circuit for adding an output of the first multiplying circuit to an output of the second multiplying circuit to obtain a carrier chrominance signal.

5. (Original) A multiple-format video encoder as claimed in claim 4, further comprising:

an inverting circuit for inverting polarity of the values of the cosine function; and

a switch for feeding the second multiplying circuit alternately with the values of the cosine function intact, for one scanning line of the RGB signals, and with the values of the cosine function after inversion by the inverting circuit, for a next line of the RGB signals, and so forth.

6. (Currently Amended) A multiple-format video encoder as claimed in claim 5,

wherein the plurality of video formats ~~format~~ used includes ~~include~~ an NTSC format and a PAL format, and

wherein, when the NTSC format is used, the switch keeps feeding the second multiplying circuit with the values of the cosine function intact, and, when the PAL format is used, the switch feeds the second multiplying circuit alternately with the values of the cosine function intact, for one scanning line of the RGB signals, and with the

values of the cosine function after inversion by the inverting circuit, for a next line of the RGB signals, and so forth.

7. (Currently Amended) A multiple-format video encoder as claimed in claim 4,

wherein the plurality of video formats includes NTSC, PAL, PAL-M, and PAL-N formats, and

the value to be added has a different value depending on whether ~~an~~ the NTSC, PAL, PAL-M, or PAL-N format is used.

8-12. (Canceled)

13. (New) A multiple-format video encoder comprising:

a luminance/color-difference signal generating circuit that receives digital RGB signals to be inputted in synchronism with clock pulses at a predetermined frequency and generates a luminance signal and a color-difference signal from the RGB signals;

a memory that stores trigonometric function values covering a predetermined number of phases at each address thereof for each of the phases and outputs a trigonometric function value stored at a designated address; and

an address calculating circuit that receives a setting signal for selecting a predetermined video format from among a plurality of video formats each having a different chrominance subcarrier frequency, the address calculating circuit calculates a value to be added based on the chrominance subcarrier frequency of the predetermined

video format selected with the setting signal, the predetermined number of phases, and the predetermined frequency of the clock pulses, and the address calculating circuit designates a next address of the memory by adding the calculated value to be added to the designated address,

wherein a composite color video signal of the predetermined video format selected with the setting signal is generated based on the color-difference signal, the luminance signal, and a trigonometric function value stored in an address designated by the address calculating circuit.

14. (New) A multiple-format video encoder as claimed in claim 2,

wherein the value selecting circuit, the adder, and the flip-flop circuit perform operations thereof by using a larger number of bits than a minimum number of bits required to express the predetermined number of phases, and

the address calculating circuit further comprises a shift circuit for dividing, through a shift operation, a value output from the flip-flop circuit to convert the value outputted from the flip-flop circuit back into a value consisting of the minimum number of bits required to express the predetermined number of phases so as to produce the next address.

15. (New) A multiple-format video encoder as claimed in claim 14,

wherein the value selecting circuit, the adder, and the flip-flop circuit perform operations thereof by using 20 bits, and

the shift circuit divides the value output from the flip-flop circuit by 1024 to convert the value output from the flip-flop circuit back into a value consisting of 10 bits so as to produce the next address.

16. (New) A multiple-format video encoder as claimed in claim 13,

wherein the value to be added is obtained by dividing a value resulting from multiplying the chrominance subcarrier frequency by the predetermined number of phases by the predetermined frequency of the clock pulses.

17. (New) A multiple-format video encoder comprising:

a luminance/color-difference signal generating circuit that receives digital RGB signals to be inputted in synchronism with clock pulses at a predetermined frequency, generates a luminance signal and a color-difference signal from the RGB signals, and feeds out the luminance and the color-difference signals;

a memory that stores trigonometric function values covering a predetermined number of phases at each address thereof for each of the phases and outputs a trigonometric function value stored at a designated address; and

an address calculating circuit that receives a setting signal for selecting a predetermined video format from among a plurality of video formats, comprising:

a value selecting circuit that divides a value resulting from multiplying the chrominance subcarrier frequency of the predetermined video format by the predetermined number of phases by the predetermined frequency of the clock pulses and outputs a result as a value to be added;

an adder that adds the value to be added to the designated address and outputs a value to be used for deciding an address to be designated;

a flip-flop circuit that temporarily stores the value output from the adder and feeds out this value in synchronism with regular clock pulses as the address to be designated;

a multiplying circuit for multiplying the color-difference signal by a trigonometric function value read from the designated address and outputting a value therefrom, and

an adder for adding the value output from the multiplying circuit to the luminance signal to generate and output a composite color video signal.

18. (New) A multiple-format video encoder as claimed in claim 17,

wherein the value selecting circuit, the adder, and the flip-flop circuit perform operations thereof by using a larger number of bits than a minimum number of bits required to express the predetermined number of phases, and

the address calculating circuit further comprises a shift circuit for dividing, through a shift operation, the value output from the flip-flop circuit to convert the value outputted from the flip-flop circuit back into a value consisting of the minimum number of bits required to express the predetermined number of phases so as to produce the address to be designated.

19. (New) A multiple-format video encoder as claimed in claim 18,

wherein the value selecting circuit, the adder, and the flip-flop circuit perform operations thereof by using 20 bits, and

the shift circuit divides the value output from the flip-flop circuit by 1024 to convert the value output from the flip-flop circuit back into a value consisting of 10 bits so as to produce the address to be designated.

Cont'd.

20. (New) A multiple-format video encoder as claimed in claim 17,

wherein the plurality of video formats includes NTSC, PAL, PAL-M, and PAL-N formats, and

the value to be added has a different value depending on whether the NTSC, PAL, PAL-M, or PAL-N format is used.